# TMS27C128
# 131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

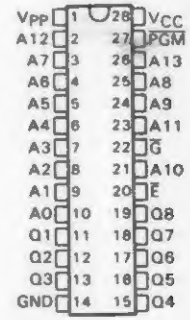
OCTOBER 1984 – REVISED NOVEMBER 1985

- Organization . . . 16K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K and 128K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

| | | |
|---|---|---|
| '27C128-1, | '27C128-15 | 150 ns |
| '27C128-2, | '27C128-20 | 200 ns |
| '27C128, | '27C128-25 | 250 ns |
| '27C128-3, | '27C128-30 | 300 ns |
| '27C128-4, | '27C128-45 | 450 ns |

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation ($V_{CC}$ = 5.25 V)
  - –Active . . . 210 mW Worst Case
  - –Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)




| PIN NOMENCLATURE | |
|---|---|
| A0-A13 | Address Inputs |
| $\overline{E}$ | Chip Enable/Power Down |
| $\overline{G}$ | Output Enable |
| GND | Ground |
| $\overline{PGM}$ | Program |
| Q1-Q8 | Outputs |
| $V_{CC}$ | 5 V Power Supply |
| Vpp | 12.5-V Power Supply |

## description

The TMS27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-onl memories. These devices are fabricated using HVCMOS technology for high speed and simple interfac with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TT circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circu without external resistors. The data outputs are three state for connecting multiple devices to a commo bus. The TMS27C128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-ir line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programmir signals are TTL level. For programming outside the system, existing EPROM programmers can be use Locations may be programmed singly, in blocks, or at random.

## operation

There are seven modes of operation for the TMS27C128 listed on the following page. Read mode requir a single 5-V supply. All inputs are TTL level except for Vpp during programming (12.5 V) and 12 V c A9 for signature mode.

**switching characteristics over full ranges of recommended operating conditions (see Note 4)**

| PARAMETER | | TEST CONDITIONS (SEE NOTES 4 AND 5) | '27C128-1 '27C128-15 | | '27C128-2 '27C128-20 | | '27C128 '27C128-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ | Access time from address | $C_L$ = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | | 150 | | 200 | | 250 | ns |
| $t_{a(E)}$ | Access time from chip enable | | | 150 | | 200 | | 250 | ns |
| $t_{en(G)}$ | Output enable time from $\overline{G}$ | | | 75 | | 75 | | 100 | ns |
| $t_{dis}$ | Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first† | | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| $t_{v(A)}$ | Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first† | | 0 | | 0 | | 0 | | ns |

| PARAMETER | | TEST CONDITIONS (SEE NOTES 4 AND 5) | '27C128-3 '27C128-30 | | '27C128-4 '27C128-45 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ | Access time from address | $C_L$ = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | | 300 | | 450 | ns |
| $t_{a(E)}$ | Access time from chip enable | | | 300 | | 450 | ns |
| $t_{en(G)}$ | Output enable time from $\overline{G}$ | | | 120 | | 150 | ns |
| $t_{dis}$ | Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first† | | 0 | 105 | 0 | 130 | ns |
| $t_{v(A)}$ | Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first† | | 0 | | 0 | | ns |

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

**recommended timing requirements for programming, $T_A$ = 25°C, $V_{CC}$ = 6 V, $V_{PP}$ = 12.5 V (see Note 4)**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(IPGM)}$ | Initial program pulse duration | 0.95 | 1 | 1.05 | ms |
| $t_{w(FPGM)}$ | Final pulse duration | 2.85 | | 78.75 | ms |
| $t_{su(A)}$ | Address setup time | 2 | | | μs |
| $t_{su(E)}$ | $\overline{E}$ setup time | 2 | | | μs |
| $t_{su(G)}$ | $\overline{G}$ setup time | 2 | | | μs |
| $t_{dis(G)}$ | Output disable time from $\overline{G}$ | 0 | | 130 | ns |
| $t_{en(G)}$ | Output enable time from $\overline{G}$ | | | 150 | ns |
| $t_{su(D)}$ | Data setup time | 2 | | | μs |
| $t_{su(VPP)}$ | $V_{PP}$ setup time | 2 | | | μs |
| $t_{su(VCC)}$ | $V_{CC}$ setup time | 2 | | | μs |
| $t_{h(A)}$ | Address hold time | 0 | | | μs |
| $t_{h(D)}$ | Data hold time | 2 | | | μs |

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and $\overline{V_{PP}}$ = 12.5 V ± 0.5 V during programming. Input and output timing reference levels are 0.8 V and 2 V.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.







TMS27C128
131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

**PARAMETER MEASUREMENT INFORMATION**

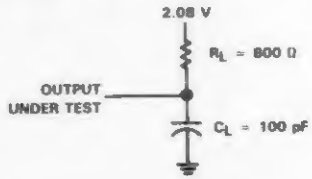
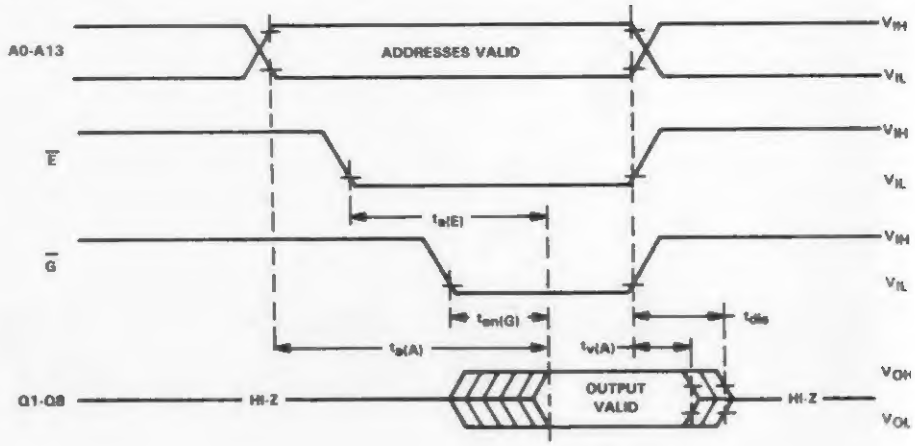


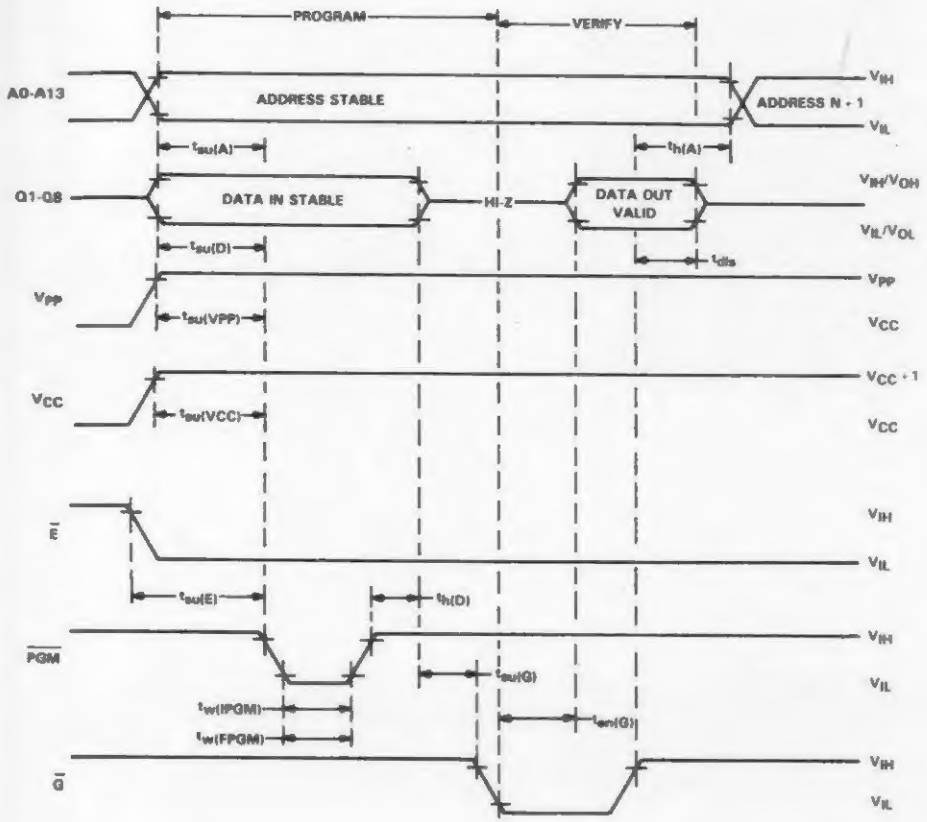

FIGURE 2. OUTPUT LOAD CIRCUIT

**read cycle timing**




TEXAS INSTRUMENTS

## program cycle timing









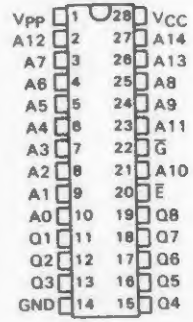

SEPTEMBER 1984 — REVISED NOVEMBER 1985

- Organization . . . 32K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 128K and 256K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

| | | |
|---|---|---|
| '27C256-1, | '27C256-17 | 170 ns |
| '27C256-2, | '27C256-20 | 200 ns |
| '27C256, | '27C256-25 | 250 ns |
| '27C256-3, | '27C256-30 | 300 ns |
| '27C256-4, | '27C256-45 | 450 ns |

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation ($V_{CC}$ = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)




| PIN NOMENCLATURE | |
|---|---|
| A0-A14 | Address Inputs |
| $\overline{E}$ | Chip Enable/Power Down |
| $\overline{G}$ | Output Enable |
| GND | Ground |
| Q1-Q8 | Outputs |
| $V_{CC}$ | 5-V Power Supply |
| $V_{PP}$ | 12.5-V Power Supply |

## description

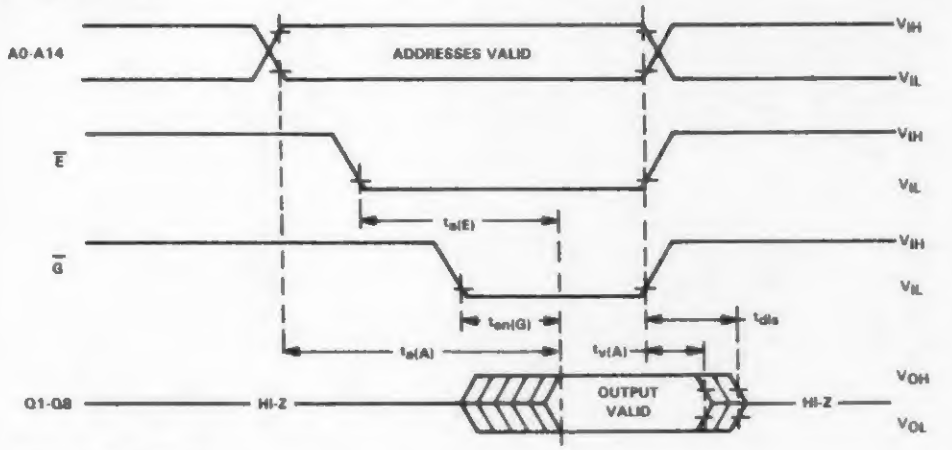
The TMS27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

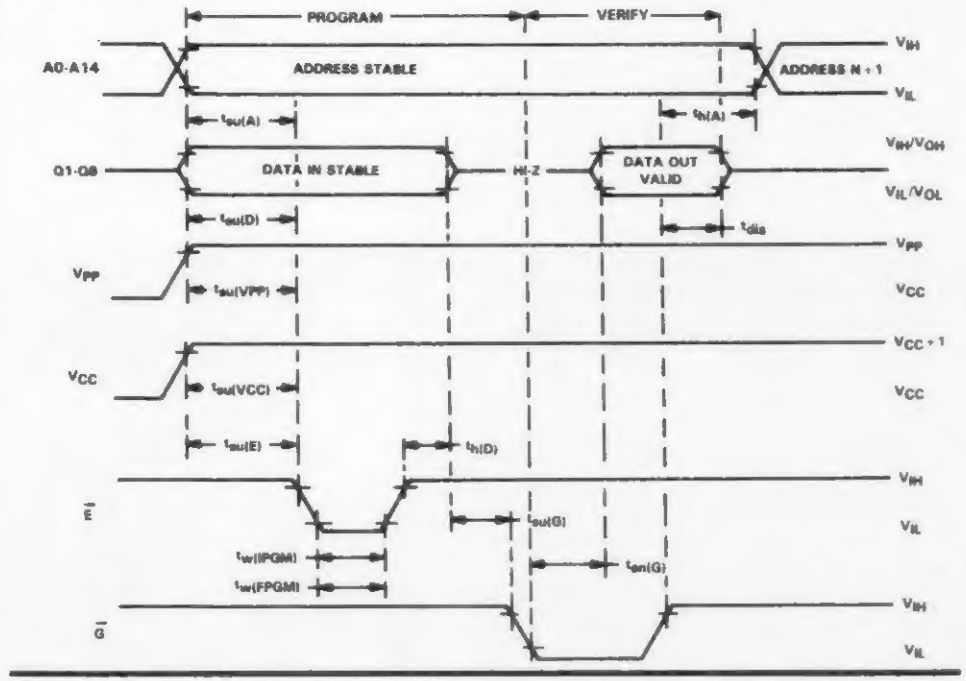
## operation

There are seven modes of operation for the TMS27C256 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for Vpp during programming (12.5 V) and 12 V on A9 for signature mode.

**read cycle timing**




**program cycle timing**






TEXAS INSTRUMENTS

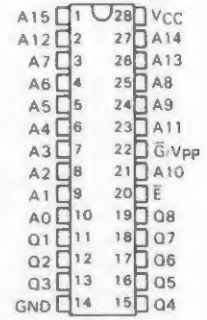


- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 512K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

| | | |
|---|---|---|
| '27C512-2, | '27C512-20 | 200 ns |
| '27C512, | '27C512-25 | 250 ns |
| '27C512-3, | '27C512-30 | 300 ns |
| '27C512-4, | '27C512-45 | 450 ns |

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation ($V_{CC}$ = 5.25 V)
  - —Active . . . 263 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)




| PIN NOMENCLATURE | |
|---|---|
| A0-A15 | Address Inputs |
| $\overline{E}$ | Chip Enable/Power Down |
| GND | Ground |
| Q1-Q8 | Outputs |
| $V_{CC}$ | 5-V Power Supply |
| $\overline{G}/V_{PP}$ | 12.5 V Power Supply/ Output Enable |

**description**

The TMX27C512 series are 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27C512 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.



TEXAS INSTRUMENTS




6 EPROMs/PROMs